PLEASE AMEND THE SPECIFICATION, PAGES 8-10

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The method consist of providing a semiconductor substrate doped with a first conductive type dopant. The substrate typically is single crystal silicon and is doped with P-type dopant, such as boron (B). A shallow trench isolation (STI) field oxide (FOX) areas is formed in and on the substrate and surrounds and electrically isolates device areas on the substrate. A thin gate oxide is formed on the device areas usually by growing a silicon oxide ($SiO_2$) layer by thermal oxidation. A conductively doped polysilicon layer is formed by depositing a polysilicon which is doped with an N-type conductive dopant. The N doped polysilicon layer is patterned to include gate electrodes over device areas. Next lightly doped source/drain areas are formed in the device areas adjacent to said gate electrodes by ion implantation, using a second conductive type dopant (N-dopant), such as arsenic ions ($As^{75}$) or phosphorus ($P^{31}$). Insulating sidewall spacers are formed on the sidewalls of the gate electrodes by depositing a conformal silicon oxide layer by chemical vapor deposition (CVD) and anisotropically plasma etching back the CVD-$SiO_2$. During the etch back, the top surface of the polysilicon gate electrodes and the source/drain contact areas are exposed. Next, optional, heavily doped source/drain contact areas are formed in the device areas adjacent to the sidewall spacers by ion

implanting a the second conductive type dopant, such as As or P. Self-aligned silicide (SALICIDE) FETs are formed next by depositing a relatively thin conformal metal layer, such as titanium (Ti) or cobalt (Co), on the substrate over the gate electrodes and the device areas. A first thermal anneal, preferably a rapid thermal anneal (RTA-1) is carried out to selectively form a silicide layer ($TiSi_x$ or a CoSix) on the top surface of the gate electrodes and on the source/drain contact areas. The unreacted metal layer on the oxide sidewall spacer and other oxide surfaces (e.g. STI) is then removed by selectively wet etching. Next, a conformal etch stop/barrier layer, composed of $Si_3N_4$ or silicon oxynitride (SiON), is deposited by CVD. An interlevel dielectric (ILD) layer, for example composed of CVD-$SiO_2$ is deposited over the etch stop layer and provides electrical insulation for the next level of electrical interconnection. The ILD layer is typically planarized. Next, borderless contact openings are etched in the ILD layer to the source/drain areas. These borderless contact openings extend over the field oxide. Typically, because of the nonuniformity of the ILD layer and the nonuniformity etch rate across the substrate it is necessary to over etch to insure that all contacts openings are open across the substrate. Unfortunately, this results in over etching the field oxide regions (STI) at the field oxide-source/drain area interface and results in source/drain-to-substrate shorts when conducting plugs, such as metal plugs, are subsequently formed in the contact

openings. Now, by the method of this invention, a contact dopant is ion implanted in the substrate under and adjacent to the over-etched field oxide regions in the borderless contact openings. The second thermal anneal, preferably a second RTA (RTA-2), is performed to complete the phase transition of the metal silicide (to reduces sheet resistance) and concurrently to active the ion implanted contact dopant to form source/drain contact areas that are continuous around the over-etched field oxide regions. This modified diffused metallurgical junction reduces the electrical shorts when conducting plugs are later formed in the borderless contact openings. Since the contact implant is integrated into the salicide FET process the thermal budget for the process is not increased, which is essential for future shallow junction devices.

PLEASE AMEND THE CLAIMS - CLEAN COPY

21. (AMENDED) A Salicide field effect transistor with improved borderless contact openings comprised of:

a semiconductor substrate doped with a first conductive type dopant and having device areas surrounded and electrically isolated shallow trench field oxide areas;

a gate oxide layer on said device areas, and a conductively doped patterned polysilicon layer doped with a second conductive type dopant over said device